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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/672,131	09/27/2000	Gary S. Kitten	M-8847 US	7081

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EXAMINER
LEE, CHRISTOPHER E

ART UNIT	PAPER NUMBER
2112	

DATE MAILED: 10/08/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/672,131	KITTEN ET AL.	
	Examiner	Art Unit	
	Christopher E. Lee	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 August 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,6-10 and 13-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,6-10 and 13-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Receipt Acknowledgement

1. Receipt is acknowledged of the request filed on 27th of August 2004 for a Request for Continued Examination (RCE) under 37 CFR 1.114 based on the Application No. 09/672,131, which the request is acceptable and an RCE has been established. Claims 1-3, 7-10 and 13-15 have been amended; no claim has been canceled; and no claim has been newly added since the RCE Final Office Action was mailed on 30th of April 2004. Currently, claims 1-3, 6-10 and 13-15 are pending in this application.

Claim Objections

2. In the claims 7 and 13-15, each of the claim status is not (original), but (currently amended). See MPEP 714 [R-2] and 37 CFR 1.121(c). Appropriate correction is required.

Claim Rejections - 35 USC § 103

3. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

4. Claims 1, 2, 6-9, 13 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Odaohhara et al. [US 6,574,740 B1; hereinafter Odaohhara] in view of Phu et al. [US 6,321,278 B1; hereinafter Phu].

Referring to claim 1, Odaohhara discloses an apparatus (i.e., computer 10 of Fig. 1) comprising: an audio controller (i.e., Audio Controller 41 of Fig. 1); a PCI bus (i.e., PCI Bus 27 of Fig. 1) connecting a PCI card slot (i.e., Slot 40 of Fig. 1) to a card/bus controller (i.e., CardBus Controller 39 of Fig. 1; See col. 7, lines 17-19); and said audio controller (i.e., Audio Controller) connected to said PCI bus (See col. 7, lines 19-21).

Odaohhara does not expressly teach a first audio input/output (I/O) connector provided for coupling to a first audio I/O device; a second audio I/O connector provided for coupling to a second audio I/O device; said first and second connectors being coupled to said audio controller; and a transistor coupled to said

first and second connectors and to ground, said transistor connected to pull said first device coupled to said first I/O connector to a zero voltage level when said second device is coupled to said second I/O connector.

Phu discloses a switching mechanism for an automatically detecting a connection into a computer system standardized connector for disabling a front speaker (See Fig. 5 and Abstract), wherein a first audio input/output (I/O) connector (i.e., line-out jack 500 of Fig. 5) provided for coupling to a first audio I/O device (i.e., external loudspeakers 104 in Fig. 1A; See col. 7, lines 60-62); a second audio I/O connector (i.e., headphone jack/switch 405 of Fig. 5) provided for coupling to a second audio I/O device (i.e., headphone 106 of Fig. 1A; See col. 6, lines 35-38); said first and second connectors (i.e., line-out jack and headphone jack/switch) being coupled to an audio controller (i.e., coupled to Sound Device 116 in Fig. 5); and a transistor (i.e., transistor switch 412 of Fig. 5) coupled to said first and second connectors and to ground (See Fig. 5 and col. 5, lines 51-65), said transistor (i.e., transistor switch) connected to pull said first device (i.e., external loudspeakers) coupled to said first I/O connector (i.e., line-out jack) to a zero voltage level (i.e., a logic "0") when said second device (i.e., headphone) is coupled to said second I/O connector (i.e., headphone jack/switch; See col. 5, line 66 through col. 6, line 7 and lines 35-60). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said switching mechanism with said transistor switch (viz., transistor) for an automatic detection/switching said connection, as disclosed by Phu, in said apparatus, as disclosed by Odaohhara, for the advantage of providing to route audio signals to various audio transducers of said apparatus (i.e., computer system), such as said audio devices (i.e., internal loudspeaker, headphone and external loudspeakers) without an interference (See Phu, col. 2, lines 6-13).

Referring to claim 8, Odaohhara discloses a computer system (i.e., computer 10 of Fig. 1), comprising: a processor (i.e., CPU 13 of Fig. 1); a memory (i.e., Main Memory 19 of Fig. 1) coupled to said processor (See col. 6, line 58 through col. 7, line 4); an audio controller (i.e., Audio Controller 41 of

Fig. 1) coupled to said processor (i.e., Audio Controller 41 being coupled to CPU 13 via PCI Bus 27 and Memory/PCI Control Chip 15 in Fig. 1); connecting a PCI bus (i.e., PCI Bus 27 of Fig. 1) to a PCI card slot (i.e., Slot 40 of Fig. 1) and to a card/bus controller (i.e., CardBus Controller 39 of Fig. 1; See col. 7, lines 17-19); and connecting said audio controller (i.e., Audio Controller) to said PCI bus (See col. 7, lines 19-21).

Odaohhara does not expressly teach a first audio I/O connector coupled to said audio controller and provided for coupling to a first audio I/O device; a second audio I/O connector coupled to said audio controller and provided for coupling to a second audio I/O device; and a transistor coupled to said first and second connectors and to ground, said transistor connected to pull said first device coupled to said first I/O connector to a zero voltage level when said second device is coupled to said second I/O connector.

Phu discloses a switching mechanism for an automatically detecting a connection into a computer system standardized connector for disabling a front speaker (See Fig. 5 and Abstract), wherein a first audio I/O connector (i.e., line-out jack 500 of Fig. 5) coupled to an audio controller (i.e., coupled to Sound Device 116 in Fig. 5) and provided for coupling to a first audio I/O device (i.e., external loudspeakers 104 in Fig. 1A; See col. 7, lines 60-62); a second audio I/O connector (i.e., headphone jack/switch 405 of Fig. 5) coupled to said audio controller (i.e., said Sound Device) and provided for coupling to a second audio I/O device (i.e., headphone 106 of Fig. 1A; See col. 6, lines 35-38); and a transistor (i.e., transistor switch 412 of Fig. 5) coupled to said first and second connectors and to ground (See Fig. 5 and col. 5, lines 51-65), said transistor (i.e., transistor switch) connected to pull said first device (i.e., external loudspeakers) coupled to said first I/O connector (i.e., line-out jack) to a zero voltage level (i.e., a logic "0") when said second device (i.e., headphone) is coupled to said second I/O connector (i.e., headphone jack/switch; See col. 5, line 66 through col. 6, line 7 and lines 35-60).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said switching mechanism with said transistor switch (viz., transistor) for an automatic detection/switching said connection, as disclosed by Phu, in said computer system, as disclosed by Odaohhara, for the advantage of providing to route audio signals to various audio transducers of said computer system, such as said audio devices (i.e., internal loudspeaker, headphone and external loudspeakers) without an interference (See Phu, col. 2, lines 6-13).

Referring to claims 2 and 9, Odaohhara teaches an I/O controller hub (i.e., Multifunction PCI Device 33 of Fig. 1) connected to said PCI bus (i.e., PCI Bus 27 of Fig. 1; See col. 7, lines 10-18).

Referring to claims 6 and 13, Phu teaches said first audio I/O connector comprises a jack (i.e., line-out jack 500 of Fig. 5).

Referring to claims 7 and 14, Phu teaches said second audio I/O connector comprises a jack (i.e., headphone jack/switch 405 of Fig. 5).

5. Claims 3, 10 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Odaohhara [US 6,574,740 B1] in view of Phu [US 6,321,278 B1] as applied to claims 1, 2, 6-9, 13 and 14 above, and further in view of Murthy [US 6,643,822 B1].

Referring to claims 3 and 10, Odaohhara, as modified by Phu, discloses all the limitations of the claims 3 and 10, respectively, including an I/O controller (i.e., I/O Controller 51 of Fig. 1; Odaohhara) connected to said I/O controller hub (i.e., Multifunction PCI Device 33 of Fig 1; Odaohhara), except that does not expressly teach said I/O controller is a super I/O controller.

Murthy discloses a computer system 100 in Fig. 6, wherein a super I/O controller (i.e., Super I/O Controller 28 of Fig. 6) connected to an I/O controller hub (i.e., Input/Output Controller Hub 22 of Fig/ 6).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have substituted said I/O controller, as disclosed by Odaohhara, as modified by Phu, by said

super I/O controller (i.e., Super I/O Controller), as disclosed by Murthy, for the advantage of performing many I/O functions including interfacing with various input and output devices (See Murthy, col. 8, lines 39-46).

Referring to claim 15, Phu teaches said first connector (i.e., line-out jack 500 of Fig. 5) and said second audio I/O connector (i.e., headphone jack/switch 405 in Fig. 5), each comprise a jack (i.e., combination jack; See Abstract).

Response to Arguments

6. Applicants' arguments with respect to claims 1 and 8 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Farrar [US 5,910,991 A] discloses method and apparatus for a speaker for a personal computer for selective use as a conventional speaker of as a sub-woofer.

Brown [US 5,822,406 A] discloses switching circuit for automatically routine audio and data signals between a modem, telephone, and I/O devices.

Iglehart et al. [US 6,091,812 A] disclose apparatus and method for automatically switching a headset between a telephone and a second audio source.

Hijii [US 6,459,911 B1] discloses portable telephone equipment and control method therefor.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christopher E. Lee whose telephone number is 703-305-5950. The examiner can normally be reached on 9:30am - 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark H. Rinehart can be reached on 703-305-4815. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Christopher E. Lee
Examiner
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